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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/945,266	COULSON, RICHARD L.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 10 is objected to because of the following informalities:

It seems that a verb is missing. Moreover, this claim does not further limit its parent claim as the limitation of this claim now appears in the independent claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4, 11, 23 – 26 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamaguchi (US Patent No. 5,386,546).

With respect to claims 1 and 32, Hamaguchi discloses a method (figure 3) comprising:

checking a current clock period when a memory is accessed (S15, time stamp), the current clock period being one of a given number of clock periods; and

setting a usage bit corresponding to the current clock period during a writeback cycle (S150, see also col. 4, lines 7 – 11, S150 writes the time stamp loaded at S15), the usage bit indicating usage information for the memory.

4. With respect to claims 4 and 34, the method further comprises:

resetting usage bits in response to changing an address/tag of the memory; and

setting a usage bit corresponding to a current clock period (old time stamp of the evicted cache entry is replaced with the time stamp of the new entry).

5. With respect to claim 11, the method further comprises:

de-allocating data in the memory based upon the usage bits if the memory is considered full (figure 3, one of the dirty cache entries is evicted, or de-allocated if the cache memory is full).

6. With respect to claims 23 – 25, 35, 38 Hamaguchi discloses a method comprising:

storing metadata comprising usage information (figure 1) for a memory wherein the usage information is a least recently used information (4); and

updating the usage information during a writeback cycle (col. 4, lines 7 – 10, new time stamp replaces the old time stamp).

7. With respect to claims 26 and 28, see rejections of claim 1 and 4, respectively.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 3, 27 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Martine *et al.* (US Patent No. 5,619,675, hereinafter "De Martine") in view of Hamaguchi.

De Martine disclose a method comprising:

checking a current clock period (figure 3, 310, 312, 314, 316) when a memory is accessed, the current clock period being one of a given number of clock periods; and

setting a usage bit (302, 304, 306, 308) corresponding to the current clock period, the usage bit indicating usage information for the memory; and

erasing usage bits corresponding to a new clock period when the new clock period begins (col. 6, lines 51 – 52, see also claim 2).

However, De Martine does not specifically disclose that the usage bits are set during a writeback cycle. On the other hand, Hamaguchi teaches that modified data in cache must be written back for data consistency (Hamaguchi, col. 4, lines 7 – 12). Hamaguchi discloses setting usage bits during a writeback cycle (see rejection of claim 1). Writeback requires access which in turn results in setting of the usage bit.

It would have been obvious to one of ordinary skill in the art, having the teachings of De Martine and Hamaguchi before him at the time the invention was made, to use the writeback of dirty cache teachings of Hamaguchi in the cache system of De Martin, in order to maintain cache coherency as not writing back of dirty data leads to data inconsistency.

10. Claims 5, 8 – 10, 12 – 14, 17 – 20, 29, 31, 37, 40 – 45, 47 – 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamaguchi in view of Davis *et al.* (US Patent Application Publication No. 2003/0023922, hereinafter "Davis").

11. With respect to claims 5 – 8 – 10, 14 – 20, 29, 31, 37, 40 – 45 and 48 Hamaguchi discloses a system comprising:

a memory to store data and metadata for the data (figure 1), the metadata including a plurality of usage bits to indicate usage information for the memory (4, 5), each usage bit corresponding to one of a given number of clock periods; and

a memory controller to update the usage bits during a writeback cycle based on the clock period and to de-allocate the data using the plurality of usage bits (figure 3B).

However, Hamaguchi does not specifically disclose a magnetic memory device or a destructive memory device to cache data. On the other hand, Davis discloses that an MRAM device, which is a magnetic destructive read memory device, is ideally suited to replace any prior art solid state device (Davis, page 6, paragraph 70).

It would have been obvious to one of ordinary skill in the art, having the teachings of Hamaguchi and Davis before him at the time the invention was made, to use the MRAM device teachings of Davis in the computer system of Hamaguchi to replace cache and the main memory with MRAM, since Davis disclose that MRAMs are ideally suited to replace any prior-solid state storage device. (Davis, page 6, paragraph 70). According to Davis, MRAM devices have relatively low power consumption and relatively fast access times (page 1, paragraph 3).

12. With respect to claim 47, the apparatus resulting from the combination of Hamaguchi and Davis discussed above would require "writeback" to rewrite data back whenever cache is read since the data read is destroyed during a read process. When broadly but reasonably interpreted, any data written back can be said to be an update since the destroyed data must be updated with the valid data to prevent erroneous results.

13. Claims 6, 15, 21 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Martine in view of Hamaguchi and Davis.

De Martine and Hamaguchi disclose all of the limitation of the independent claim 1. Davis disclose non-volatile magnetic destructive read cache memory as discussed above with the resulting combination disclosing all of the limitation of the parent claims.

In addition, De Martine discloses that the given number of clock periods is four (figure 3).

14. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blaner *et al.* (US Patent No. 6,157,981, hereinafter "Blaner") in view of Yamamoto *et al.* (US Patent No. 5,444,651, hereinafter "Yamamoto").

Blaner discloses a memory (figure 1, see also claim 1) to cache data for a storage device and to store usage information (102, 106, effective address to derive the physical address of data, or where in the physical memory this data is used) for the cache data stored in the memory. However, Blaner does not specifically disclose that the cache memory is of non-volatile destructive type. On the other hand, Yamamoto disclose a polymer ferroelectric memory, which is a non-volatile destructive read memory.

It would have been obvious to one of ordinary skill in the art, having the teachings of Blaner and Yamamoto before him at the time the invention was made, to use the ferroelectic memory teachings of Yamamot in the cache system of Blaner, since Blaner discloses that the cache memory may be of any type (Blaner, col. 2, lines 61 – 64). Yamamoto's non-volatile memory is adapted for use in a computer (Yamamoto, col. 1, lines 14 – 16).

Conclusion

15. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
April 11, 2005

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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